CLAIMS

What is claimed is:

1. An identification circuit for establishing and sensing the state of a fusible element used in on chip type identification comprising:

a circuit establishing control signals for enabling the identification circuit for sensing with an initiating signal, which signal remains off during a personalization of the fusible element;

dual paths energized by said control signals generated by a level setting circuit to energize one path through the fusible element to provide a state level and another path through a reference path that provides a reference voltage level that is distinguishable from both the blown and unblown states of the fusible element;

a differential sensing circuit for comparing said reference voltage level to said state level to provide a signal indicating a state of the fusible element; and

protection circuitry changing voltage levels on said dual paths and said differential sensing circuit to protect said circuit during an operation in which the state of the fusible element is set.

2. The identification circuit of claim 1 wherein,

said reference path includes a resistive element to form said reference voltage level wherein said resistive element is formed with substantially equivalent material as said fusible element.

3. The identification circuit of claim 1 including a fusible element personalization circuit to establish the state of the fusible element.

4. The identification circuit of claim 3 wherein, the personalization circuit includes a personalizing FET and a source of potential capable of fusing the fusible element arranged in series with the fusible element; and

a NOR circuit controlling the personalization FET responsive to the presence or absence of a blow signal to establish the state of the fusible element.

5. The identification circuit of claim 4 wherein,

the fusible state and reference paths are each a series circuit that includes switching devices responsive to the control signals for making and breaking the reference paths and isolation devices in series with the switching devices to isolate them and other circuit chip elements from the fusible element while the fusible element is being personalized.

6. The identification circuit of claim 3 including coupling and decoupling devices to connect and disconnect the dual paths to the differential sensing circuit to the dual paths.

7. The identification circuit of claim 6 wherein,

the coupling and decoupling devices includes one coupling device for coupling one input terminal of the differential sensing circuit to the fusible element path and another coupling device for coupling the reference path to another input terminal of the differential sensing circuit to the reference path during sensing the state of fusible element.

8. The identification circuit of claim 6 wherein,

the coupling and decoupling devices includes two FET devices each for connecting one of the input terminals of the differential sensing circuit to ground during personalization of the fusible element.

9. The identification circuit of claim 3 including a latching circuit coupled to the differential sensing circuit for retaining the sensed state of the fusible element.

10. The identification circuit of claim 9 wherein,

said latching circuit is a stage in a shift register for shifting the sensed state of the fusible element off the semiconductor chip.

11. A circuit for controlling the state of a fusible element used in a semiconductor chip comprising:

a circuit establishing control signals for enabling the circuit for sensing with an initiating signal which signal remains off during establishing the state of the fusible element;

dual paths energized by said control signals generated by a state setting circuit to energize one path through the fusible element to provide a state level and another path through a reference path that provides a reference voltage level that is distinguishable from both the blown and unblown states of the fusible element;

a differential sensing circuit for comparing said reference voltage level to said state level to provide a signal indicating the state of the fusible element; and

protection circuitry changing voltage levels on said dual paths and the differential sensing circuit to protect the circuit during an operation in which the state of the fusible element is set.

12. The circuit of claim 11 wherein,

said reference path includes a resistive element to form said reference voltage level wherein said resistive element is formed with substantially equivalent material as said fusible element.

13. The circuit of claim 11 including a fusible element personalization circuit to establish the state of the fusible element.

14. The circuit of claim 13 wherein, the personalization circuit includes a personalizing FET and a source of potential capable of fusing the fusible element arranged in series with the fusible element; and

a NOR circuit controlling the personalization FET responsive to the presence or absence of a blow signal to establish the state of the fusible element.

15. The circuit of claim 14 wherein,

the fusible state and reference paths are each a series circuit that includes switching devices responsive to the control signals for making and breaking the reference paths and isolation devices in series with the switching devices to isolate them and other circuit chip elements from the fusible element while the fusible element is being personalized.

16. The circuit of claim 12 including coupling and decoupling devices to connect and disconnect the dual paths to the differential sensing circuit to the dual paths.

17. The circuit of claim 16 wherein,

the coupling and decoupling devices includes one coupling device for coupling one input terminal of the differential sensing circuit to the fusible element path and another coupling device for coupling the reference path to another input terminal of the differential sensing circuit to the reference path during sensing the state of fusible element.

18. The circuit of claim 16 wherein,

the coupling and decoupling devices includes two FET devices each for connecting one of the input terminals of the differential sensing circuit to ground during personalization of the fusible element.

19. The circuit of claim 13 including a latching circuit coupled to the differential sensing circuit for retaining the sensed state of the fusible element.

20. The circuit of claim 19 wherein,

said latching circuit is a stage in a shift register for shifting the sensed state of the fusible element off the semiconductor chip.